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L7	1	(soc and ebiu).clm.	US-PGPUB	OR	ON	2009/07/31 12:44
L8	5	(soc and (test adj bench)).clm.	US-PGPUB	OR	ON	2009/07/31 12:44
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L2	45	soc and verif\$7 and ((test adj bench) or testbench) and @pd>= "20081101"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2009/07/31 12:27
L5	58	(international adj business adj machine).as. and soc and verif\$7 and @pd<= "20020101"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2009/07/31 12:38

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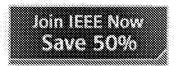
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Chou, E.; Sheu, B.;

Circuits and Devices Magazine, IEEE

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AbstractPlus | Full Text: PDF(491 KB) | IEEE JNL

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Using a soft core in a SoC design: experiences with p

Dey, S.; Panigrahi, D.; Li Chen; Taylor, C.N.; Sekar, K.; Sanchez, P.;

Design & Test of Computers, IEEE

Volume 17, Issue 3, July-Sept. 2000 Page(s):60 - 71

Digital Object Identifier 10.1109/54.867896

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Г

Г

3. Design verification and DFT for an embedded reconfi multiplier in system-on-chip applications

Margala, M.; Xianling Chen; Jian Xu; Hongfan Wang;

ASIC/SOC Conference, 2001. Proceedings. 14th Annual IEEE International

12-15 Sept. 2001 Page(s):230 - 234

Digital Object Identifier 10.1109/ASIC.2001.954703

AbstractPlus | Full Text: PDF(288 KB) | IEEE CNF

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IP reuse in the system on a chip era

Savage, W.; Chilton, J.; Camposano, R.; System Synthesis, 2000. Proceedings. The 13th International Symposium on 20-22 Sept. 2000 Page(s):2 - 7 Digital Object Identifier 10.1109/ISSS.2000.874022 AbstractPlus | Full Text: PDF(720 KB) IEEE CNF Rights and Permissions

Г 5. Design and verification of a stack processor virtual co

Stadler, M.; Thalmann, M.; Rower, T.; Kaeslin, H.; Felber, N.; Fichtner, W.; Micro, IEEE Volume 21, Issue 2, March-April 2001 Page(s):69 - 80

Digital Object Identifier 10.1109/40.918004

AbstractPlus | Full Text: PDF(300 KB) | IEEE JNL

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6. Using codesign techniques to support analog function

Wolff, F.G.; Knieser, M.J.; Weyer, D.J.; Papachristou, C.A.; Hardware/Software Codesign, 1999. (CODES '99) Proceedings of the Sevent

3-5 May 1999 Page(s):79 - 83

Digital Object Identifier 10.1109/HSC.1999.777397

AbstractPlus | Full Text: PDF(412 KB) | IEEE CNF

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7. System-level test bench generation in a co-design fra

Łajolo, M.; Rebaudengo, M.; Sonza Reorda, M.; Violante, M.; Lavagno, L.; European Test Workshop, 2000, Proceedings, IEEE 23-26 May 2000 Page(s):25 - 30 Digital Object Identifier 10.1109/ETW.2000.873775 AbstractPlus | Full Text: PDF(416 KB) IEEE CNF

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8. A survey of digital design reuse

Jacome, M.F.; Peixoto, H.P.; Design & Test of Computers, IEEE Volume 18, Issue 3, May-June 2001 Page(s):98 - 107 Digital Object Identifier 10.1109/54.922806 AbstractPlus | Full Text: PDF(112 KB) IEEE JNL

П 9. A framework for object oriented hardware specification and synthesis

Kuhn, T.; Oppold, T.; Winterholer, M.; Rosenstiel, W.; Edwards, M.; Kashai, Y Design Automation Conference, 2001. Proceedings 2001 Page(s):413 - 418

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^{10.} A new paradigm for very flexible SONET/SDH IP-mod

Rower, T.; Stadler, N.; Thalmann, M.; Kaeslin, H.; Felber, N.; Fichtner, W.; Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEI 21-24 May 2000 Page(s):533 - 536

Digital Object Identifier 10.1109/CICC.2000.852724

AbstractPlus | Full Text: PDF(356 KB) | IEEE CNF

Rights and Permissions

11. Crossroads for mixed-signal chips

Levin, P.L.; Ludwig, R.; Spectrum, IEEE Volume 39, Issue 3, March 2002 Page(s):38 - 43 Digital Object Identifier 10.1109/6.988703 AbstractPlus | Full Text: PDF(421 KB) IEEE JNL Rights and Permissions

12. A new design cost model for the 2001 ITRS

Kahng, A.B.; Smith, G.;
Quality Electronic Design, 2002. Proceedings. International Symposium on 18-21 March 2002 Page(s):190 - 193
Digital Object Identifier 10.1109/ISQED.2002.996728

AbstractPlus | Full Text: PDF(211 KB) | IEEE CNF Rights and Permissions

^{13.} A "design for verification" methodology

Sforza, F.; Battu, L.; Brunelli, M.; Castelnuovo, A.; Magnaghi, M.; Quality Electronic Design, 2001 International Symposium on 26-28 March 2001 Page(s):50 - 55
Digital Object Identifier 10.1109/ISQED.2001.915205
AbstractPlus | Full Text: PDF(576 KB) | IEEE CNF Rights and Permissions

^{14.} RT-level ITC'99 benchmarks and first ATPG results

Corno, F.; Reorda, M.S.; Squillero, G.;

Design & Test of Computers, IEEE

Volume 17, Issue 3, July-Sept. 2000 Page(s):44 - 53

Digital Object Identifier 10.1109/54.867894

AbstractPlus | Full Text: PDF(124 KB) IEEE JNL

Rights and Permissions

^{15.} C-based SoC design flow and EDA tools: an ASIC and perspective

Wakabayashi, K.; Okamoto, T.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 19, Issue 12, Dec. 2000 Page(s):1507 - 1522
Digital Object Identifier 10.1109/43.898829

AbstractPlus | Full Text: PDF(388 KB) | IEEE JNL
Rights and Permissions

16. Codesign paradigm in digital/analog tradeoffs

Wolff, F.G.; Knieser, M.J.; Weyer, D.J.; Papachristou, C.A.;
ASIC/SOC Conference, 1999. Proceedings. Twelfth Annual IEEE Internations
15-18 Sept. 1999 Page(s):76 - 80
Digital Object Identifier 10.1109/ASIC.1999.806478

AbstractPius | Full Text: PDF(372 KB) IEEE CNF
Rights and Permissions

Г 17. Enhanced reusability for SoC-based HW/SW co-desig Boden, M.; Schneider, J.; Feske, K.; Rulke, S.; Digital System Design, 2002. Proceedings. Euromicro Symposium on 4-6 Sept. 2002 Page(s):94 - 99 Digital Object Identifier 10.1109/DSD.2002.1115356 AbstractPlus | Full Text: PDF(305 KB) IEEE CNF Rights and Permissions 18. VHDL-based simulation environment for Proteo NoC Siguenza-Tortosa, D.; Numi, J.; High-Level Design Validation and Test Workshop, 2002. Seventh IEEE Intern 27-29 Oct. 2002 Page(s):1 - 6 AbstractPlus | Full Text: PDF(497 KB) | IEEE CNF Rights and Permissions 19. A layered approach to behavioral modeling of bus pre-Chonnad, S.; Needamangalam, B.; ASIC/SOC Conference, 2000. Proceedings, 13th Annual IEEE International 13-16 Sept. 2000 Page(s):170 - 173 Digital Object Identifier 10.1109/ASIC.2000.880696 AbstractPlus | Full Text: PDF(268 KB) IEEE CNF Rights and Permissions 20. Essential issues for IP reuse _ Gajski, D.D.; Wu, A.C.-H.; Chaiyakul, V.; Mori, S.; Nukiyama, T.; Bricaud, P.; Design Automation Conference, 2000, Proceedings of the ASP-DAC 2000, A 25-28 Jan. 2000 Page(s):37 - 42 Digital Object Identifier 10.1109/ASPDAC.2000.835067 AbstractPlus | Full Text: PDF(376 KB) IEEE CNF Rights and Permissions П 21. Hardware-software co-design of embedded systems : N2C methodology for application development Tsasakou, S.; Voros, N.S.; Koziotis, M.; Verkest, D.; Prayati, A.; Birbas, A.; Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99. The 6th I Conference on Volume 1, 5-8 Sept. 1999 Page(s):59 - 62 vol.1 Digital Object Identifier 10.1109/ICECS.1999.812222 AbstractPlus | Full Text: PDF(224 KB) | IEEE CNF Rights and Permissions 22. Teaching future verification engineers: the forgotten design Ozguner, F.; Marhefka, D.; DeGroat, J.; Wile, B.; Stofer, J.; Hanrahan, L.; Design Automation Conference, 2001, Proceedings 2001 Page(s):253 - 255 AbstractPlus | Full Text: PDF(280 KB) | IEEE CNF Rights and Permissions

How VSIA answers the SOC dilemma

Birnbaum, M.; Sachs, H.;
Computer
Volume 32, Issue 6, June 1999 Page(s):42 - 50
Digital Object Identifier 10.1109/2.769442

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²⁴ Multiprocessor SoC platforms: a component-based d

Cesario, W.O.; Lyonnard, D.; Nicolescu, G.; Paviot, Y.; Sungjoo Yoo; Jerraya Nava, M.;
Design & Test of Computers, IEEE
Volume 19, Issue 6, Nov.-Dec. 2002 Page(s):52 - 63
Digital Object Identifier 10.1109/MDT.2002.1047744

AbstractPlus | Full Text: PDF(327 KB) | IEEE JNL
Rights and Permissions

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Bradley, D.W.; Tyrrell, A.M.;
Evolutionary Computation, IEEE Transactions on
Volume 6, Issue 3, June 2002 Page(s):227 - 238
Digital Object Identifier 10.1109/TEVC.2002.1011538
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H Chang, L Cooke, M Hunt - 1999 - books.google.com

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S Dey, D Panigrahi, L Chen, CN Taylor, K ... - IEEE Design & **Test** of computers, 2000 - ieeexplore.ieee.org ... core can be integrated in an **SoC** design, the ... the picoJava core, the user must **verify** the core at ... Therefore, we had to modify the **test-bench** environment of the ...

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M Birnbaum, H Sachs, FM Inc - Computer, 1999 - ieeexplore.ieee.org ... An **SOC**'s gate count can be very large, and it ... are being established to simulate and **verify** this new ... Behavioral models Emulation model Evaluation **test bench** ... Cited by 60 - Related articles - BL Direct - All 6 versions

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W Savage, J Chilton, R Camposano - Proceeding of 13 th International Symposium on ..., 2000 - doi.ieeecomputersociety.org

... and actively work against the success of SoC technology by ... the test bench into the other language and verify the test vectors pass the new test bench. ...

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PDFI ► C-based SoC design flow and EDA tools: An ASIC and system vendor perspective K Wakabayashi, T Okamoto - IEEE Transactions on Computer-Aided Design of ..., 2000 - icdesign4fun.com ..., and semi-formal veri- fiers, and test-bench generators. ... level sim- ulations and directly verify their circuit ... WAKABAYASHI AND OKAMOTO: C-BASED SOC DESIGN FLOW ... Cited by 75 - Related articles - View as HTML - BL Direct - All 5 versions

A framework for object oriented hardware specification, verification, and synthesis- **> ethz.ch**

T Kuhn, T Oppold, M Winterholer, W ... - Proceedings of the 38th conference on Design ..., 2001 - portal.acm.org ... A key aspect of **verifying SoC** designs, which ... allows the designer to specify, **verify**, and synthesize ... synthesis which may facilitate **test bench** acceleration and ... Cited by 35 - Related articles - All 19 versions

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DS Brahme, S Cox, J Gallo, M Glasser, W ... - Cadence Design Systems, Inc, 2000 - masters.donntu.edu.ua ... A system-on-a-chip (SoC) for Voice-over ... gen- erators and checkers to verify design functionality ... Test bench creation continues until test plan requirements have ...

Cited by 39 - Related articles - View as HTML - All 7 versions

RTL C-based methodology for designing and verifying a multi-threaded processor-

dac.com (PDF)

L Semeria, A Seawright, R Mehra, D Ng, A ... - Design Automation Conference, 2002. Proceedings. ..., 2002 -

ieeexplore.ieee.org

... RTL equivalence checking tool [1,8,11,13] is used to **verify** the syn ... thesized netlist are also verified using co-simulation with the C **test-bench** environment. ...

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Verification of configurable processor cores- ▶ psu.edu [PDF]

M Puig-Medina, G Ezer, P Konas - Proceedings of the 37th conference on Design ..., 2000 - portal.acm.org ..., 4. A **TEST-BENCH** FOR **SOC** VERIFICATION in order to **verify** a configured Xtensa processor we build a system emulation **test-bench** around the processor (Figure 4). ...

Cited by 19 - Related articles - BL Direct - All 13 versions

The changing landscape of system-on-a-chip design

AM Rincon, WR Lee, M Slattery, IBM ... - Custom Integrated Circuits, 1999. Proceedings of the ..., 1999 - ieeexplore.ieee.org

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